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# Channel Temperature Analysis of GaN HEMTs with Nonlinear Thermal Conductivity

Ali M. Darwish, Andrew Bayba, and H. Alfred Hung

***Abstract*—This paper presents an enhanced, closed-form expression for the thermal resistance, and thus, the channel temperature of AlGaN/GaN HEMTs, including the effect of temperature-dependent thermal conductivity of GaN and SiC or Si substrates. Additionally, the expression accounts for temperature increase across the die-attach. The model's validity is verified by comparing it with experimental observations. The model results also compare favorably with those from finite-element numerical simulations across the various device geometric and material parameters. The model provides a more accurate channel temperature than that from a constant thermal conductivity assumption; this is particularly significant for GaN/Si HEMTs where the temperature rise is higher than in GaN/SiC. To our knowledge, this paper presents the first reliable, analytical model for predicting the channel temperature with nonlinear thermal conductivities. It is especially useful for device and MMIC designers in the thermal assessment of their device design iterations against required performance for their specific applications.**

***Index Terms*—Wide Bandgap, GaN, AlGaN, HEMT, Thermal Resistance, non-linear thermal conductiviey, Reliability.**

## I. Introduction

THE reliability and power performance of semiconductor devices depend on the operating channel temperature. In Gallium Nitride (GaN) devices the potential for temperature related degradation is more critical given the high power density involved. In GaN HEMTs, bias voltages range from 20 – 48 V, and saturation current is typically 1 A/mm, compared with 7 – 10 V and 0.5 A/mm for nominal GaAs pHEMTs. This leads to power densities which are almost an order of magnitude higher, resulting in significant localized heat generation. In nominal, thermally-limited device characterizations, it is typical to predict excellent power densities for large devices based on small device measurements [1]-[3], with low self heating, and then observe a significant reduction [4] for the larger device, due temperature induced performance degradation. This underscores the need for a dependable temperature estimation method. The availability of an analytical expression for the channel temperature would provide the designer with a time-efficient iterative tool such that device layout optimization can occur early in the design process. It would also provide a means for assessing reliability prior to fabrication. An analytical expression for calculating the thermal resistance was previously presented [5]. However, it does not account for the temperature dependence of the thermal conductivity of GaN and the substrate material. The assumption of constant thermal conductivity may not hold for recently improved, high-power devices where the temperature increases are significant. This is of particular concern with GaN/Si HEMTs where the temperature rise is higher than in GaN/SiC.

A number of experimental and numerical approaches have been used for channel temperature characterization in GaN HEMTs including electrical measurement techniques [6]-[7], three-dimensional finite element (FE) simulation [8], scanning thermal microscopy [9], thermo-reflectance thermo-graphy [10], infrared microscopy [11], and micro-Raman [12]. In general, FE simulations give very accurate quantitative answers, provided the HEMT details (layers, thicknesses, quality of interfaces, etc.) are fully known, which is sometimes challenging. Experimental techniques apply to existing devices only, have varying levels of resolution and accuracy, and require, in most cases, specialized equipment. Both experimental and simulation techniques such as FE are indispensible. Analytical models can complement them by providing time-efficient, qualitative assessments with sufficient accuracy during the iterative design process.

In this paper, an enhanced closed-form expression for channel temperature is presented. The model accounts for the nonlinear thermal conductivity of GaN and the substrate material by employing Kirchhoff's transformation. It also includes the die-attach thermal resistance, which is significant. Several restrictions may limit the accuracy of Kirchhoff's transformation. First, the transformation's theory was developed for a single layer substrate problem. Its application to a single layer substrate is well proven [13]. The nonlinear nature of the present problem means that superposition (adding $\Delta T$ for each layer) is invalid, unless the nonlinearity effect, for each leayer, is not dominant. Second, for the transformation to be valid, the boundary conditions should be either isothermal (constant $T$ surface), or have a fixed , where $x$ represents the length dimension. Both of these conditions are not completely met at the GaN/substrate interface. Third, the transformation is valid, strictly speaking, for

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materials with isotropic thermal conductivity only. However, the thermal conductivity of SiC is anisotropic; there is a 20-30% difference in thermal conductivity between the 'a-axis' and the 'c-axis' of the crystal. A common workaround has been to measure an average (or equivalent isotropic) thermal conductivity, and treat SiC as an isotropic material. Typical thermal conductivities reported in the literature are isotropic-equivalent values. Fourth, the accuracy of the model in [5] was only tested against predicting the *total* temperature rise, in low power density (hence, linear) cases. The temperature rise, in [5], across *each* layer (GaN and substrate) was not verified and applying Kirchhoff's transformation for each layer will produce inaccurate results if $\Delta T$ for *each* layer is not correct. Given the above limitations, one should verify, experimentally and numerically, the application of Kirchhoff's transformation to the multi-layer structure at hand before using it. (NOTE: may need to tone down limitation of our previous work)

In this work, it is shown that the transformation can be applied successfully to a *two-layer* GaN thermal model - together with a third layer, the die-attach, by using sequential iterative transformations. The validity of the new approach is methodically verified by comparisons with extensive simulation and experimental results. The results from the current expression compare favorably with those from FE simulations, using ANSYS [14], and with experimental data of micro-Raman measured devices [12]. The work presents a GaN-specific, analytical nonlinear temperature model, which can be incorporated into commercial CAD software programs.

## II. PROBLEM DEFINITION AND SOLUTION

Consider a HEMT with a constant highly localized heat sources (Fig. 1) on a GaN layer of thickness $t_{GaN}$, and a substrate of thickness $t_{Sub}$.

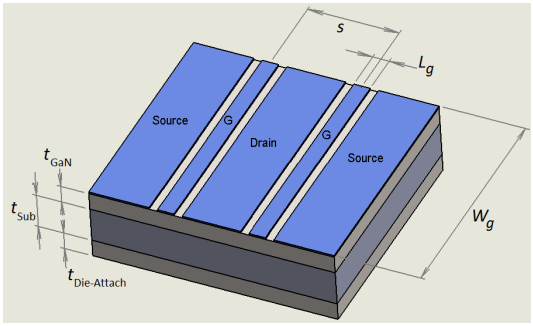


Fig. 1. HEMT geometric parameters. Gate parameters are $L_g$ x $W_g$, and gate to gate spacing $s$. Only 2 gates of a device are depicted here, but decive can have a number of gates.

The gates of the device represent heat sources, $W_g$ is the gate width, $L_g$ is the gate length, and $s$ is the gate pitch.

An expression for the thermal resistance, assuming constant thermal conductivity, was previously developed [5]. It was derived based on the solution of Laplace's equation in prolate spheroidal and cylindrical coordinates. Based on the previous formulation, one can write a new enhanced expression for the temperature rise, and account for additional effects such as those from the die-attach,

$$\Delta T = \Delta T_{GaN} + \Delta T_{Sub} + \Delta T_{Die-attach} \tag{1}$$

where the temperature rise in the GaN epitaxial layer is $\Delta T_{GaN}$, in the substrate layer is $\Delta T_{Sub}$, and in the die-attach is $\Delta T_{Die\text{-}attach}$, which are given by,

$$\Delta T_{GaN}(T_o) = \frac{P_{mm}}{\pi\, k_{GaN}(T_o)} \ln\left(\frac{4\, t^*_{GaN}}{\pi \rho L^*_g}\right) \tag{2}$$

$$\Delta T_{Sub}(T_o) = \frac{P_{mm}}{\pi\, k_{Sub}(T_o)} \ln\left(\frac{f\left(1/2\, t^*_{GaN}\right)}{f\left(\sqrt{1+(1/s^*)^2-(t^*_{GaN}/s^*)^2}\right)}\right) + \frac{\sqrt{2}\, P_{mm}}{\pi\, s^*\, k_{Sub}(T_o)} \ln\left(\frac{h\left((1/t^*_{Sub})^2-(2t^*_{GaN}/t^*_{Sub})^2\right)}{h\left((1/s^*)^2-(2t^*_{GaN}/s^*)^2\right)}\right) \tag{3}$$

$$\Delta T_{Die-attach} = P_{diss}\, t_{Die-attach} / k_{Die-attach}\, A_{Die-attach} \tag{4}$$

where,

$$f(x)=\frac{\sqrt{x+1}+\sqrt{x-1}}{\sqrt{x+1}-\sqrt{x-1}} \quad h(x)=\sqrt{\frac{\sqrt{x+1}+1}{\sqrt{x+1}-1}}$$
$$t_{GaN}^{*}=\frac{\rho t_{GaN}}{W_g} \quad t_{Sub}^{*}=\frac{\pi t_{Sub}}{W_g} \quad s^{*}=\frac{s\sqrt{2}}{W_g} \quad L_g^{*}=\frac{L_g}{W_g} \tag{5}$$
$$P_{mm}=\frac{P_{diss}}{NW_g} \quad \rho=4k_{GaN}/\pi^2 k_{Sub}$$

where $N$ is the number of gate fingers, $T_o$ is a reference temperature, $P_{diss}$ is the total dissipated power, $P_{mm}$ is the dissipated power density (in Watts per *mm* of gate width), $t_{\mathrm{GaN}}$ is the GaN thickness, $t_{\mathrm{Sub}}$ is the substrate thickness, $k_{\mathrm{GaN}}$ is the GaN thermal conductivity, $k_{\mathrm{Sub}}$ is the substrate thermal conductivity, $\Delta T_{\text{Die-attach}}$ is the temperature increase across the die-attach material, $t_{\text{Die-attach}}$, and $A_{\text{Die-attach,}}$ are the thickness and area of die-attach material, respectively.

The enhanced expression presented in this new form reveals an interesting observation. Namely, the gate width $W_{\mathrm{g}}$, does not appear explicitly in equations (2) – (5). Instead, it is a normalizing factor for all other parameters ($L_{\mathrm{g}}$, $s$, $P_{diss}$, $t_{\mathrm{GaN}}$, and $t_{\mathrm{Sub}}$). This is similar to the microstrip-line characteristic impedance expression where the substrate height ($h$) is a normalizing factor and what matters is the ratio of $W/h$, where $W$ is the line width. Thus, one should not consider $W$, and $h$ to be two independent variables. Instead, their ratio is used as an independent variable. This facilitates, in the case of microstrip lines, scaling the thickness of the microstrip substrate up and down without changing the characteristic impedance or effective dielectric constant. Similarly, in the FET/HEMT heating problem, the gate finger width can be scaled up and down while maintaining the same temperature, as long as the normalized parameters are kept constant. Stated differently, increasing (decreasing) the gate finger width is equivalent to decreasing (increasing) all the other parameters, in the same proportion.

Next, the expression will be modified to account for the temperature dependence of the thermal conductivity using Kirchhoff's transformation. This transformation has been employed earlier [15]-[18] to single layer structures (e.g. GaAs HEMTs, etc.). However, it has not been applied to a two-layer semiconductor structures such as GaN on SiC or GaN on Si. In [16], the Kirchhoff's transformation was applied to a single-layer for GaN on SiC using Cook's thermal model [19]. Cooke's model has been shown to lack accuracy [13] and applies to single layer problems; hence, the GaN layer was ignored in [16]. Although the GaN layer is thin (typically 1 μm) compared with the substrate (typically 100 μm), its contribution is nontrivial as will be shown.

Generally, the dependence of thermal conductivity on temperature is given in the form,

$$k(T)=k_{To}\left(\frac{T}{T_o}\right)^{-\alpha} \tag{6}$$

where α is a constant, $k_{To}$ is the thermal conductivity at temperature $T_o$, and $T$ is the operating temperature. For phonon-phonon interactions in a perfect crystal α is 1 [20]. Alpha differs from 1 for the materials of interest here due to scattering from point defects, which has been studied by several researchers [21]-[28]. The heat equation may be solved using Kirchhoff's transformation [15] to give,

$$T_{non-lin}(\Delta \mathrm{T}_{\mathrm{lin}},T_o,\alpha)=T_o\left(1+(1-\alpha)\left(\frac{\Delta \mathrm{T}_{\mathrm{lin}}}{T_o}\right)\right)^{\frac{1}{1-\alpha}} \tag{7}$$

where $\Delta T_{\mathrm{lin}}$ is the linear thermal temperature increase, and $T_{non\text{-}lin}$ is the temperature accounting for thermal conductivity nonlinearity.

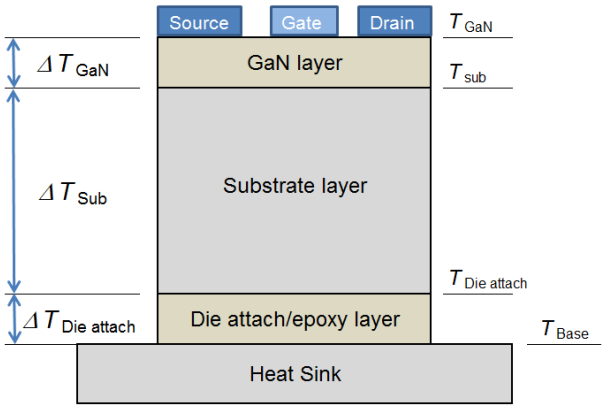


Fig. 2. Cross section of HEMT showing the temperature rise across layers.

Based on the preceding consideration, one can summarize the calculation procedure as follows. The channel temperature of the device equals the base temperature ($T_{\text{Base}}$), plus the temperature rise across the die-attach material ($\Delta T_{\text{Die-attach}}$), plus the temperature rise across the substrate ($\Delta T_{\text{Sub}}$), SiC for example, plus the temperature rise across the GaN layer ($\Delta T_{\text{GaN}}$), see Fig. 2. Equation (4) can be used to find $\Delta T_{\text{Die-attach}}$. The temperature rise across the substrate $\Delta T_{\text{Sub}}$ is given by Eq. (3). However, in calculating $\Delta T_{\text{Sub}}$, one should set $T_o = T_{\text{Base}} + \Delta T_{\text{Die-attach}}$. To account for the substrate temperature-dependent thermal conductivity, one should apply (7), with $\Delta T_{lin} = \Delta T_{Sub}$. This will give the actual operating temperature $T_{\text{Sub}}$ at the substrate/GaN interface. Finally, the temperature rise across the GaN layer $\Delta T_{\text{GaN}}$, can be calculated from (2) with $T_o = T_{\text{Sub}}$, followed by application of (7), with $\Delta T_{lin} = \Delta T_{GaN}$. The procedure of calculating the channel temperature $T_{\text{GaN}}$ may be carried out in the following computational order, using equations (2) - (7),

$$T_{Die-attach} = \Delta T_{Die-attach} + T_{Base} \tag{8}$$

$$\Delta T_{Sub} = \Delta T_{Sub}(T_{Die-attach}) \tag{9}$$

$$T_{Sub} = T_{Die-attach}\left(1+(1-\alpha_{Sub})\left(\frac{\Delta T_{\text{Sub}}}{T_{Die-attach}}\right)\right)^{\frac{1}{1-\alpha_{Sub}}} \tag{10}$$

$$\Delta T_{GaN} = \Delta T_{GaN}(T_{Sub}) \tag{11}$$

$$T_{GaN} = T_{Sub}\left(1+(1-\alpha_{GaN})\left(\frac{\Delta T_{\text{GaN}}}{T_{Sub}}\right)\right)^{\frac{1}{1-\alpha_{GaN}}} \tag{12}$$

In the following sections the results of this approach will be compared with those from simulations and experiments.

## III. VERIFICATION OF MODEL VS. SIMULATIONS

One of the accurate means of calculating thermal resistance, heat flux, and temperature is through the use of FE simulation; however, it is a time-consuming process. To verify the model, ANSYS [14] FE software was used. The element shape selected was tetrahedral and highly refined meshing was performed to ensure the accuracy of the results. Very close agreement is observed between ANSYS and the model.

The accuracy of the model for real, operational devices depends on the correctness of the thermal conductivities, $k_{To}$, of the materials employed. The conductivity of GaN is the most varied in the literature, and is attributed to the type and quantity of crystal defects [21]-[25]. In the present study, the quadratic model of Heller [29] was used. This model is based on the experimental findings of Liu and Balandin [24], the results of which were fitted to equation (6), the standard form. The thermal conductivities of SiC and Si that we apply are the commonly used values. However, the reader can verify all values with their own research and make any appropriate modification to the values of $k_{To}$ and α. In all of the calculations, the following thermal conductivities of GaN, SiC, and Si, are used,

$$k_{GaN}(T) = 1.65\left(\frac{T}{300}\right)^{-0.49} \ W/cm\cdot K \tag{13}$$

$$k_{SiC}(T) = 3.74\left(\frac{T}{300}\right)^{-1.49} \; W/cm\cdot K \quad [14] \tag{14}$$

$$k_{Si}(T) = 1.48\left(\frac{T}{300}\right)^{-1.3} \; W/cm\cdot K \quad [17] \tag{15}$$

Figs. 3a, 3b, 3c, 3d, 3e, and 3f show the comparison between the model and ANSYS simulations as $t_{Sub}$, $L_g$, $W_g$, $s$, $P_{diss}$, and $T_{Base}$ are varied, respectively. The following default parameters are used: $t_{Si} = t_{SiC} = 100$ µm, $t_{GaN} = 1$ µm, $L_g = 0.25$ µm, $W_g = 250$ µm, $s = 25$ µm, $T_o = 25$ °C, $P_{mm} = 5$ W/mm, and source/drain/gate metal thickness of 1 µm is used in ANSYS. The parameters were varied across a wide range of practical situations. Extensive simulations showed similar agreement between the model and ANSYS as $t_{Sub}$, $L_g$, $T_{Base}$, and $t_{GaN}$, are varied. Close agreement (within a few percent) is observed between the model and FE simulations. In all cases, the dotted lines are drawn indicating predictions of the previously published *linear* model for both Si and SiC substrates. The dashed line is the result from the non-linear model for Si, and the solid line is the result from the non-linear model for SiC. The circles (○) are the ANSYS simulations for Si, and the squares (□) are the simulations for SiC.

Fig. 3g shows a comparison of the temperature rise predicted by the current model (solid line), ANSYS FE simulation (square), and Ref. [16] (dashed line), for the particular device analyzed in [16]. The current model and ANSYS temperature are roughly 50% higher than that predicted by [16], where the GaN layer was ignored.

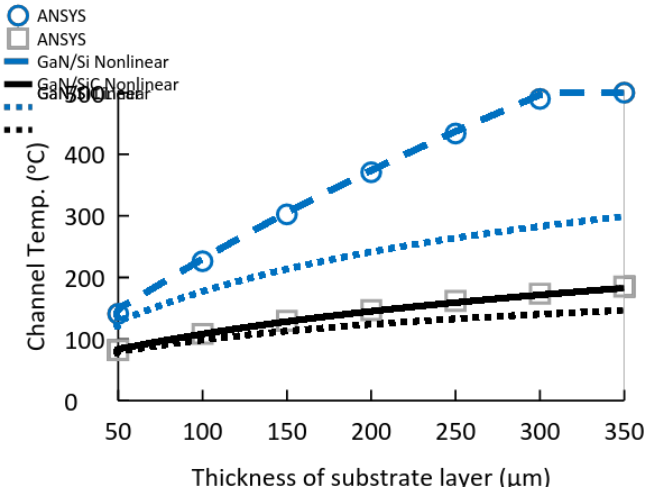


Fig. 3a. Dependence of channel temperature on SiC and Si substrate thickness ($t$) for several practical thicknesses.

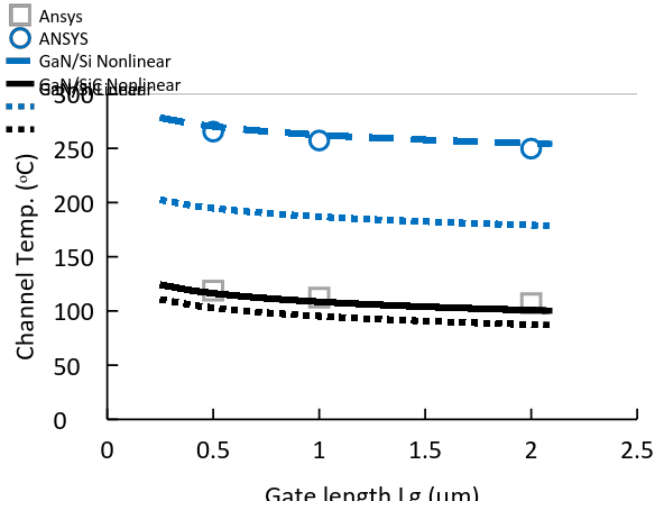


Fig. 3b. Dependence of channel temperature on gate length ($Lg$) for several practical values.

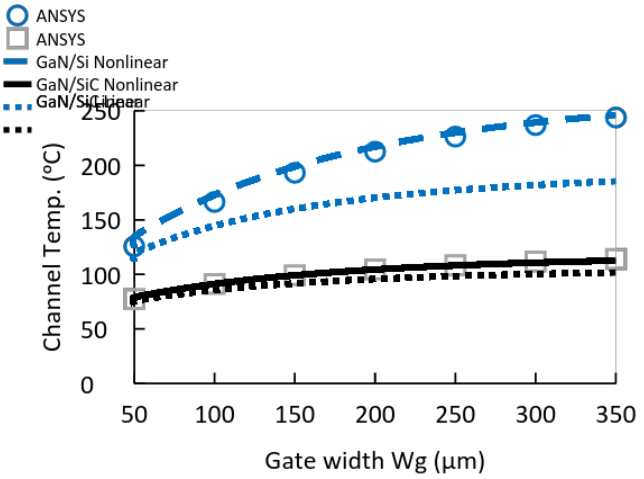


Fig. 3c. Dependence of channel temperature on gate width (*Wg*) for several practical widths.

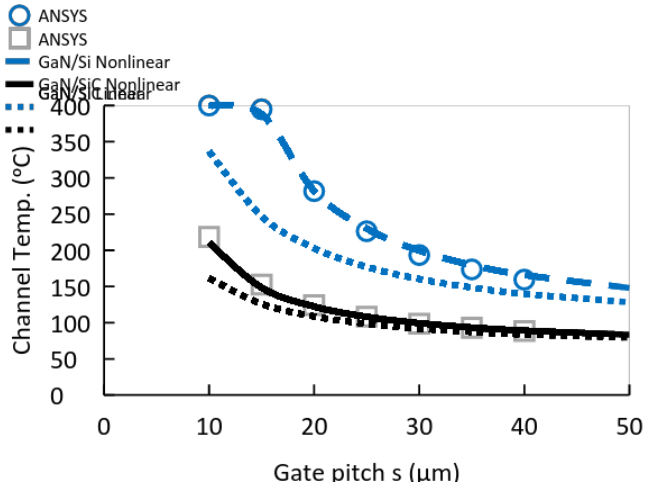


Fig. 3d. Dependence of channel temperature on gate pitch (*s*) for several practical spacing values, assuming $t = 100$ µm.

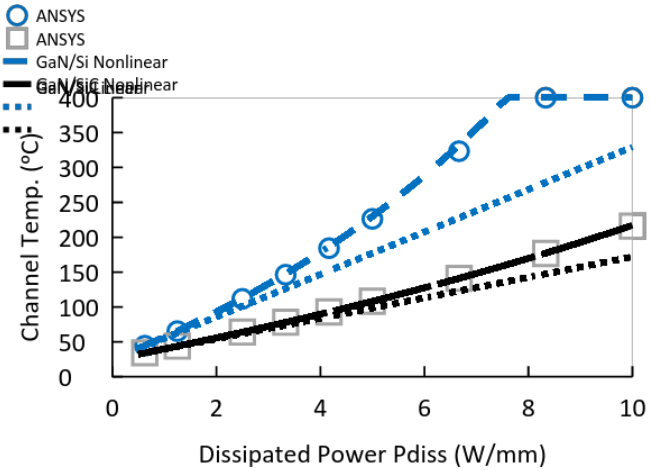


Fig. 3e. Dependence of channel temperature on dissipated power.

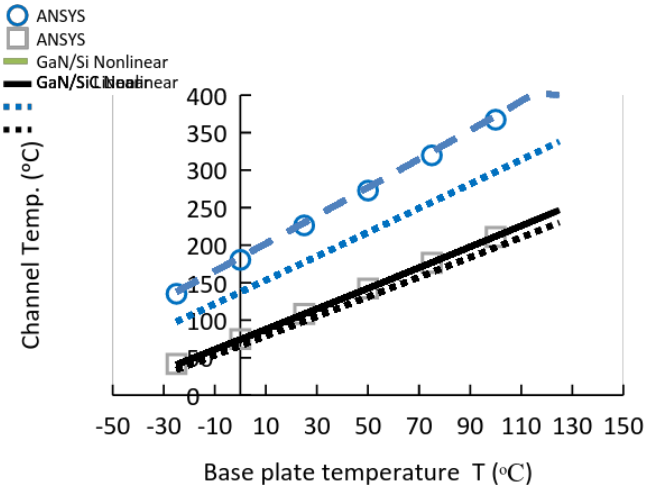


Fig. 3f. Dependence of channel temperature on base-plate temperature.

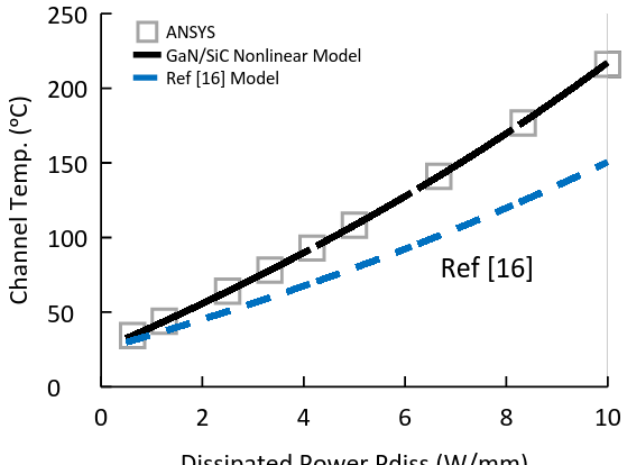


Fig. 3g. Dependence of channel temperature on dissipated power.

From the figures, it is clearly evident that the greater the channel temperature rise, the greater the linear model deviates from the correct values. The results from the linear and nonlinear models converge at low power dissipation (small temperature rise), as expected. The difference between the linear and nonlinear model is much greater for Si substrates, compared with SiC, given the latter's excellent thermal conductivity. In fact, except at low power dissipation, use of the linear model for GaN/Si is highly discouraged. It should be noted that when an Si substrate is used, the channel temperature can quickly reach unsafe temperatures with certain device structures and operating conditions. To avoid this situation, device modification such as wider gate pitches (Fig. 3d), thinner substrate, and lower power densities (Fig. 3e), could be used. For example, in the case analyzed in Fig. 3a, thinning the Si substrate from 100 μm to 50 μm reduces the temperature from 226 °C to 141 °C.

## IV. COMPARISON WITH EXPERIMENT

The best way to test the validity of a model is to compare its predicted results against accurate experimental data. However, direct measurement of channel temperature is difficult due to the infinitesimal region of the channel, and the significant temperature gradients next to the gate. In infrared microscopy (e.g. InfraScope from Quantum Focus Instruments), the spatial resolution is wavelength-limited and the technique involves spraying the device with a known emissivity substance to facilitate measurement. Clearly, the operation of the device can be affected by the substance. Micro-Raman techniques appear to be more suitable, having a significantly finer spatial resolution, and their results will be used to compare with those from the model calculations. Micro-Raman's special resolution is good but is still a limiting factor in measuring peak temperatures under the gate as will be addressed. In the present study, thermal resistance data from [30] will be compared with results from the current model. The following device parameters were used: gate pitch is 25 μm, gate length is 0.8 μm, gate width is 250 μm, number of gates is 8, substrate thickness is 350 μm, thermal conductivity is given by (13), and (14), total power input is 20V x 670 mA, and base heating is 20% of peak temperature.

The measured and calculated values are shown in Fig. 4. The calculated data agrees with the measured data but are consistently higher, as expected, because the Raman measurement is limited by the spatial resolution of the laser spot size, about 1 μm² with 2 μm in depth, and is offset from the edge of the gate. The temperature drops rapidly away from the gate due to the significant temperature gradients next to the gate edge. The temperature averaging effect in micro-Raman will always produce measured values which are lower than the actual peak values. In addition, the measured values have about 10ºC margin of error. To provide a better comparison to the micro-Raman measurements, the effect of spatial averaging should be included in the calculation; see Appendix for details of how spatial averaging is computed. Fig. 4 shows the comparison of the same measured data with spatial averaging applied to the calculated values. With spatial averaging, much closer agreement is observed. As can be seen, the effects of special averaging are significant. In this case, the calculated maximum temperature is reduced by 29% when special averaging is applied.

The model is also compared with micro-Raman measurements from [12]. Several device sizes were measured 6 × 100 μm, 12 × 100 μm, and 14 × 280 μm. The relevant details are: gate length is 0.25 μm, gate pitch is 32 μm, measurement resolution is 0.75 μm, GaN layer thickness is 2 μm, substrate thickness is 100 μm, eutectic thickness is 38 μm, and chip area is 0.5 × 0.5 mm². Fig. 5 shows the comparison between model and measurement results. Again, the calculated values incorporate the effect of spatial averaging. Close agreement is observed between the measured and calculated results. As a note, if the GaN layer contribution is ignored, as in [16], the previous results would be lower by 25% or more; the GaN layer contribution can be estimated from Eqs. (11), and (12).

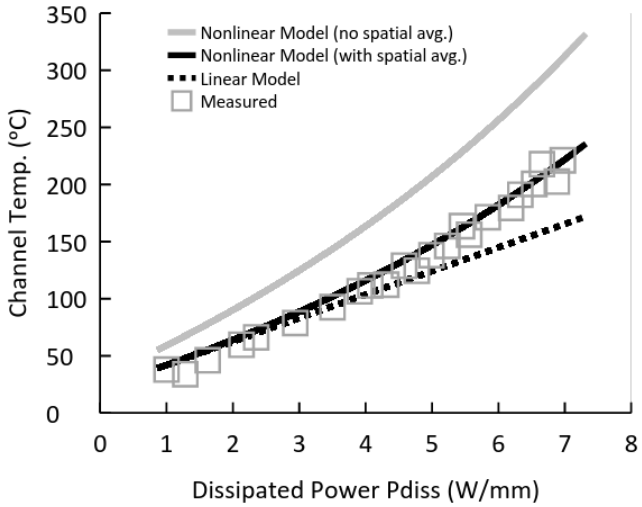


Fig. 4. Channel temperature comparison between measured (squares), calculated/linear (dotted line), calculated/nonlinear with no spatial averaging (solid gray line), and calculated/nonlinearwith spatial averaging (solid black line) for 8 × 250 μm HEMT.

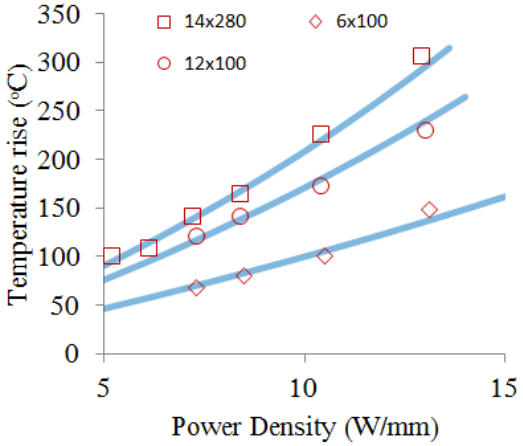


Fig. 5. Channel temperature comparison between measured (squares, circles, and diamonds), and nonlinearly calculated (solid line) for 6 × 100, 12 × 100, and 14 × 280 μm HEMTs, respectively. Spatial averaging is taken into account in the calculation.

## V. DISCUSSION

It is of significant interest that the application of Kirchhoff's transformation can provide significant results for the present non-linear case. The present work verified that the application of the Transformation for GaN/SiC and GaN/Si devicesproduces acceptable results. Additionally, it showed that in comparing simulation/theoretical results with micro-Raman measurements, spatial averaging should be considered.

There are other factors that can affect the channel temperature but presently not included in the model. Most significantly, thick metallization (for gate, source, and drain) reduce the channel temperature by providing an alternate thermal path. The model and simulations account for a thin layer (~ 1 μm) of gold metallization. Another factor which acts in the opposite direction and increases the temperature is the thermal interface resistance (or thermal boundary resistance) between GaN and the substrate [31]-[32]. This factor may or may not be significant depending on the quality of the interface, and the heat flow cross-sectional area (strongly influenced by HEMT layout geometry. Another effect which is not included is the temperature rise caused by various thin layers (hetero-junction epi-layers forming the 2DEG, thin GaN nucleation layer and/or other layers.). However, the metallization effect, anisotropy effect, thermal boundary resistance effect, and hetero-junction layers effect, are typically second order effects and may partially cancel each other.

A promising substrate material for GaN is diamond [33]. The current model should be useful in the assessment of GaN on diamond, given that the thermal boundary and interface layer resistance are low [34] ?????.

## VI. CONCLUSION

An analytical model is presented for the thermal resistance of AlGaN/GaN that includes the effects of the temperature dependence of thermal conductivity of GaN, the host substrate, and the die-attach layer. Excellent agreement has been obtained between the model and extensive ANSYS numerical simulations, across various variables. In addition, the model was verified by comparing its results with experimental data. Again, close agreement is observed considering the inherent spatial averaging which reduces the measured channel temperatures below the actual device values.

One of the findings, based on this model, is that GaN on Si may experience large temperature increases, leading to the necessity of using a model with non-linear thermal conductivity for accurate channel temperature prediction. Even in the case of a SiC substrate, accounting for the nonlinear effect is important at high power dissipation levels, as the advancing of the GaN technology will increase the demand for devices with high power density. The closed-form expression model can readily be extended to other substrates by following the same approach. With the new analytical expression, power devices and MMICs can be optimized rapidly for channel temperature assessment, and reliability improvement.

## VII. APPENDIX

In micro-Raman measurements, the laser is focused on a small volume near the gate finger. The laser's focus, according to Maxwell's equations, is a Gaussian beam with a 'beam waist' that cannot be focused to spot size below a wavelength in diameter, roughly. If spatial averaging is to be calculated accurately, one should take the Gaussian spatial distribution of the laser beam into account. However, in most cases, a reasonable estimate may be derived from assuming a uniform spatial distribution of the laser beam. To investigate the behavior of temperature as the measurement is moved away from the gate edge, ANSYS was used to simulate the case in [30]. The temperature profile predicted by FE analysis is plotted in Fig. 6.

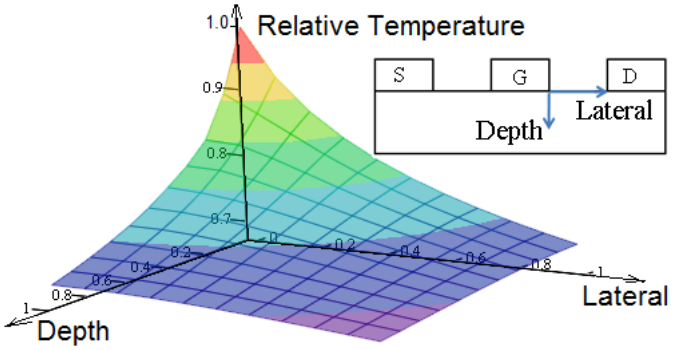


Fig. 6. Spatial distribution of relative temperature drop as one moves laterally and perpendicularly away from the gate. The plot is showing the data for 1 μm offset in either direction.

As the Figure indicates, the temperature drops rapidly with small offsets in vertical or lateral directions. The spatially averaged relative temperature ratio over a 0.7 × 0.7 μm spot is about 0.8 (applicable to Fig. 5), and over a 1 $\mu m^2$ spot with 2 μm depth is about 0.71 (applicable to Fig. 4). Hence, the temperature rise calculated by the nonlinear model should be multiplied by the proper spatial averaging factor for comparison with micro-Raman results.

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